

Phase-Synchronization Early Epileptic Seizure Detector VLSI Architecture

Karim Abdelhalim, Vadim Smolyakov, Roman Genov
 Department of Electrical and Computer Engineering
 University of Toronto, Toronto, Canada
 Email: {karim, svadim, roman}@eecg.utoronto.ca

Abstract—A low-power VLSI processor architecture that computes in real time the magnitude and phase-synchronization of two input neural signals is presented. The processor is a part of an envisioned closed-loop implantable microsystem for adaptive neural stimulation. The architecture uses three CORDIC processing cores that require shift-and-add operations but no multiplication. The 10-bit processor synthesized and prototyped in a standard 1.2V 0.13 μ m CMOS technology utilizes 41,000 logic gates. It dissipates 3.6 μ W per input pair, and provides 1.7kS/s per-channel throughput when clocked at 2.5MHz. The power scales linearly with the number of input channels or the sampling rate. The efficacy of the processor in early epileptic seizure detection is validated on human intracranial EEG data.

Index Terms—Early seizure detection, bivariate digital signal processing, biomedical processor, bivariate processing, phase-synchronization, energy-band extraction.

I. INTRODUCTION

OVER 50 million people worldwide suffer from epilepsy. Approximately one-third of those with epilepsy do not react well to currently available pharmacological treatments such as antiepileptic drugs [1]. Electrical stimulation has shown positive results in reducing the frequency of seizures in such patients with refractory epilepsy [1], [2]. Typically, the stimulation pulses are applied continuously and periodically, which can result in suboptimal treatment efficacy, shorten the battery life, increase the size of the device and increase the cost of the therapy as additional surgical operations are required for battery replacement [2]. Automated identification of optimal time instances when an electrical stimulus should be applied can help address these issues [3], [4]. In many cases, seizures can be detected prior to the clinical onset of the seizure. It has been widely hypothesized that anticipation of ictal events (i.e., seizures) is critically important for a proper control of seizures [5], [6]. This is based on the assumption and some evidence [7], [8] that it is easier to stop a seizure by electrical stimulation before or early in its development than when it has already fully developed.

Over the last two decades, extensive research has been conducted on prediction and early detection of seizures using a variety of different methods. Univariate algorithms, which involve computations on a single input, have been used to predict seizures. Such methods include computing wavelet transforms [4], energy of signal bands [9], correlation dimensions [10] and computing the Lyapunov exponent [11]. These univariate algorithms lack spatial specificity because

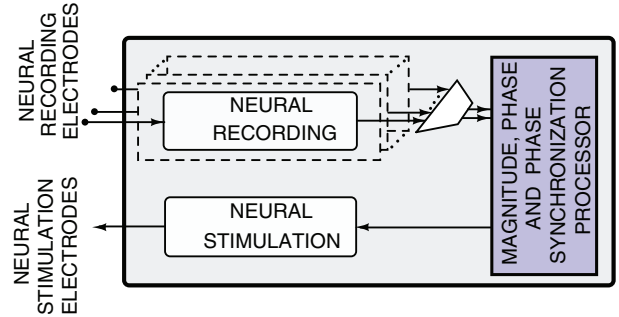


Fig. 1. Closed-loop neural recording and stimulation system for epileptic seizure detection and control.

they only rely on one recording. This issue can be addressed through bivariate or multivariate algorithms which operate on two or more inputs, respectively [12]. Seizure prediction and detection algorithms that use bivariate or multivariate measures to quantify synchronization among two or more neural signals have been shown to yield superior accuracy [5], [13], [14].

Neurons initiate electrical oscillations that are contained in multiple frequency bands such as alpha (8-12Hz), beta (13-30Hz) and gamma (40-80Hz) and have been linked to a wide range of cognitive and perceptual processes [15]. It has been shown that before and during a seizure the amount of synchrony between these oscillations from neurons located in different regions of the brain changes significantly [5]. Thus, the amount of synchrony between multiple neural signals is a strong indicator in predicting or detecting seizures [5], [13]. To quantify the level of synchrony between two neural signals, a phase locking value (PLV) can be computed that accurately measures the phase-synchronization between two signal sites in the brain [5], [16].

Existing VLSI systems that perform signal processing on neural signals typically employ univariate algorithms. These involve computations on a single input, such as computing spike thresholds [17], correlation integrals [18], autoregressive parameters [19], extracting energy bands [20], RMS, maximum-minimum, line-length and nonlinear energy [21] and analog wavelet filtering [4]. More computationally intensive techniques that use inputs from multiple recording sites such as computing the phase-synchronization, the correlation index and the similarity index between neural signals, have been used to develop more accurate seizure prediction and

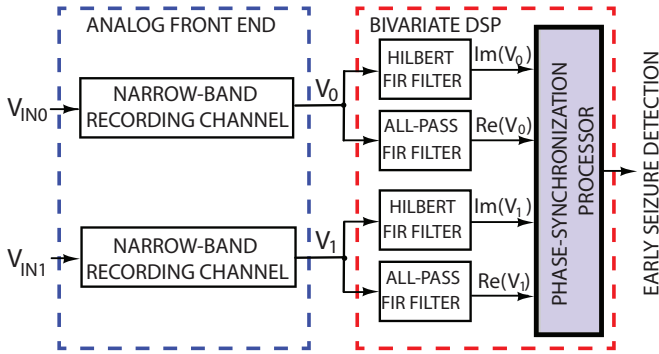


Fig. 2. Top-level block diagram of two analog neural recording channels and the digital phase-synchronization epileptic early seizure detector.

detection algorithms [5], [13], [16], [22], [23], [24], but to date have only been implemented in software.

We present a low-power digital phase-synchronization processor VLSI architecture that efficiently performs computationally intensive phase-locking value (PLV) estimation. This paper extends on an earlier report of the principle and demonstration in [25], and offers a more detailed analysis of the architecture and seizure prediction sensitivity results in human EEG data. The VLSI architecture employs the Coordinate Rotation Digital Computer (CORDIC) algorithm [26]. The algorithm offers a hardware-efficient approach to computing trigonometric and vector functions, as it requires only shift-and-add operations for vector rotations. The VLSI architecture is to be integrated with neural recording and stimulation circuits [27] to implement a multi-channel implantable closed-loop microsystem as shown in Figure 1. The phase synchronization processor combines three CORDIC processor cores, which operate on vectors to compute the magnitude, phase and the phase-synchronization of two signals. The rest of the paper is organized as follows. Section II discusses the phase-synchronization algorithm. Section III presents the VLSI architecture of the processor. Section IV describes its VLSI implementation. Section V contains simulation and experimental results of early seizure detection by the phase-synchronization processor, in human EEG recordings.

II. PHASE-SYNCHRONIZATION ALGORITHM

For two oscillations, V_0 and V_1 , when their instantaneous phase difference is locked to a constant value, synchronization is present between the two signals. A number of methods exist that quantify the level of frequency-specific synchronization between two neuroelectric signals, including mutual information and Shannon entropy [16]. Estimation of phase locking has emerged as a popular leading method of quantifying neural synchronization. Its effectiveness comes from the fact that it relies on the phase information of a neural signal, separately from its magnitude. Thus, to quantify the amount of phase locking between two neural signals requires the computation of the phase difference followed by the computation of a phase locking index. First, the Hilbert transform is applied to both signals V_0 and V_1 to compute their real and imaginary

components,

$$V_0 = \text{Re}(V_0) + j\text{Im}(V_0), \quad V_1 = \text{Re}(V_1) + j\text{Im}(V_1) \quad (1)$$

where V_0 and V_1 are two sinusoidal continuous or discrete-time signals. The Hilbert transform is conventionally performed over the full band of frequencies in the neural spectrum, and thus, a narrow-band bandpass filter should be applied before the Hilbert transform to isolate the signal band of interest [16].

The magnitude in the extracted frequency band can be computed as

$$\text{MAG}(V_k) = \sqrt{(\text{Re}(V_k))^2 + (\text{Im}(V_k))^2} \quad (2)$$

where $k=0,1$. Next, the instantaneous phases are computed for each channel

$$\phi_k = \arctan \frac{\text{Im}(V_k)}{\text{Re}(V_k)} \quad (3)$$

and if phase-synchronization exists between the two channels in the same frequency band then the difference in phase is equal to a constant

$$\Delta\phi = \phi_1 - \phi_0 = \text{constant}. \quad (4)$$

Numerous statistical tools exist that quantify the level of phase-synchronization between two signals such as entropy index, mutual information index and mean phase coherence [5]. The hardware-efficient mean phase coherence in [5] was selected, which uses a phase locking value (PLV) between 0 and 1 to evaluate the amount of phase-synchronization. The algorithm defines PLV as

$$\text{PLV} = \frac{1}{N} \sqrt{\left(\sum_{i=0}^{N-1} \sin(\Delta\phi_i) \right)^2 + \left(\sum_{i=0}^{N-1} \cos(\Delta\phi_i) \right)^2} \quad (5)$$

where N is the length of the moving-average FIR filters and $\Delta\phi_i$ is the instantaneous phase difference between the i -th samples of the two signals.

In summary, the PLV computation requires the Hilbert transform, arctan, addition, sine and cosine, moving-average filtering and lastly, the PLV magnitude. The arctan, sine/cosine and magnitude operators will be computed using the CORDIC algorithm while the moving-average filtering will be computed using digital FIR filtering. Both the magnitude value in (2) and the PLV value in (5) are used in this work for early detection of epileptic seizures.

III. VLSI ARCHITECTURE

The architecture of the feedforward path of the system in Figure 1 for two channels is presented in Figure 2 and contains both analog and digital components. After low-noise amplification of the neural signals by a low-power neural amplifier, narrow-band filter extracts the signal in the frequency band of interest.

The proposed analog front-end utilizes two stages of AC-coupled amplifiers with a gain of 1000V/V (60dB), and tuneable low-pass and high-pass filters to maintain a bandwidth between 0.1Hz and 5kHz. The capacitive feedback architecture minimizes area and power dissipation allowing

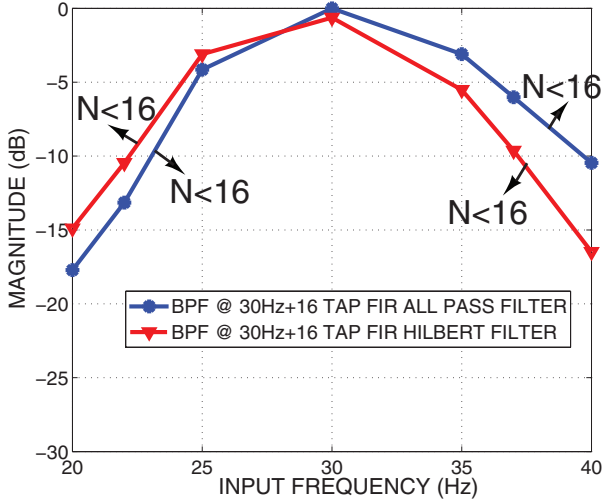


Fig. 3. Simulation results showing gain mismatch for two 16-tap FIR filters programmed for all-pass and Hilbert response (N =number of taps) with an analog bandpass filter at 30Hz.

for a large number of channels as was previously reported in [27] and [28]. The input-referred noise integrated over a 5kHz bandwidth is below $10\mu\text{V}$. A fully differential architecture minimizes common-mode noise.

A bandpass filter is required as changes in magnitude and instantaneous phase and phase difference occur in specific signal bands [15]. Narrowband synchronization outperforms broadband synchronization in recognizing the start of a seizure onset [16]. Utilizing the narrow bandwidth also puts less constraint on the input-referred noise and resolution of the analog front-end and ADC, respectively, leading to smaller area and lower power dissipation. A 2nd order analog bandpass filter with a Q of 5 was used to extract the signal band of interest.

The bandpass filtered signal is then digitized by a low-power medium resolution analog-to-digital converter (ADC). Next, each digitized signal is fed to a set of two 10-bit finite impulse response (FIR) filters. One FIR filter is configured to perform the Hilbert transform to shift the signal by 90 degrees, while the other FIR filter is an all-pass filter to ensure the digital delays of the two FIR filters are matched. To further save power, this FIR filtering can also be efficiently performed in the mixed-signal VLSI domain by incorporating it within the ADC [29]. This is why the front-end FIR filtering is not considered as a part of the phase-synchronization processor. With the high- Q bandpass filter, a FIR filter with 16 taps achieves a well matched magnitude response when programmed with the coefficients for the all-pass and Hilbert response. Further decreasing the number of taps of the FIR filters leads to gain mismatches between the all-pass and Hilbert filters as shown in Figure 3.

The rest of the computation is efficiently performed in the digital domain by using the CORDIC algorithm. Sampling more than one pair of analog channel outputs within a single seizure prediction time window yields multivariate signal processing [30].

A. CORDIC Algorithm

Next, the phase locking value is computed using the CORDIC algorithm. The CORDIC algorithm has been demonstrated in a large number of applications, such as matrix computations (QRD and eigenvalue estimation), image processing (DCT) and digital communications (FFT, DDS) [26]. The CORDIC algorithm operates on a vector of complex numbers by multiplying it by powers of two removing the requirement of complex multipliers and utilizing only adders, shifters and memory retrieval operations [26]. Using an iterative approach, CORDIC provides a high-accuracy, low-power and low-area computational algorithm at the cost of reduced speed. Two modes were implemented in CORDIC: the rotational mode which is used for computing sine and cosine, and the vectoring mode which is used to compute the magnitude and the phase. The two modes only differ in the directions of rotation [26].

The CORDIC algorithm involves iterations on three difference equations as follows

$$\text{for } n = 1 : 16 \quad (6)$$

$$x[n+1] = x[n] + y[n]2^{-(n-1)}$$

$$y[n+1] = y[n] - \text{sign}(y[n])x[n]2^{-(n-1)}$$

$$z[n+1] = z[n] + \text{sign}(y[n])\arctan(2^{-(n-1)})$$

To compute the magnitude and the phase using CORDIC, the initial values must first be set. For the CORDIC equations, the initial $x[1]$ and $y[1]$ would represent the real and imaginary components of the signal, respectively, with $y[1]$ set to 0. Over the next 16 clock cycles the procedure that computes magnitude and phase is repeated while y converges to 0. The final value $x[16]$ represents a scaled magnitude and the final value $z[16]$ represents the phase. A look-up table that stores 16 arctan values was used in the phase computation. Computing sine and cosine is similar except we initialize $x[1]$ to the CORDIC aggregate constant K , set $y[1]$ to 0 and set $z[1]$ to the angle we want to compute. Also z converges to 0 instead of y and the final output, $x[16]$, represents the cosine of the angle, while $z[16]$ represents the sine of the angle.

B. CORDIC-based Processor VLSI Architecture

The VLSI architecture of the 10-bit phase-synchronization and magnitude processor is shown in Figure 4. It uses three pipelined CORDIC cores and two moving-average FIR filters. The pipelined architecture allows the supply voltage to be lowered to minimize power dissipation by using a lower frequency clock while maintaining a constant throughput. The first core receives the two digitized vectored signals, preprocesses them by extracting the quadrant of the angle and then simultaneously computes both the angle between 0 and 90 degrees and the magnitude using a 16-bit CORDIC core configured in the vectoring mode. The angles are re-adjusted using the stored quadrant information to output an angle between 0 and 360 degrees. The difference between the two computed angles is transferred to the next stage.

The sine and cosine of the angle difference are computed using a 16-bit CORDIC core configured in the rotational mode. The computed sine and cosine as well as the negative flags

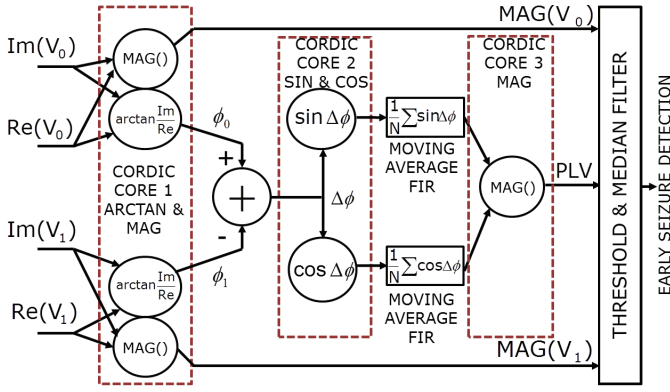


Fig. 4. VLSI architecture of the phase-synchronization processor.

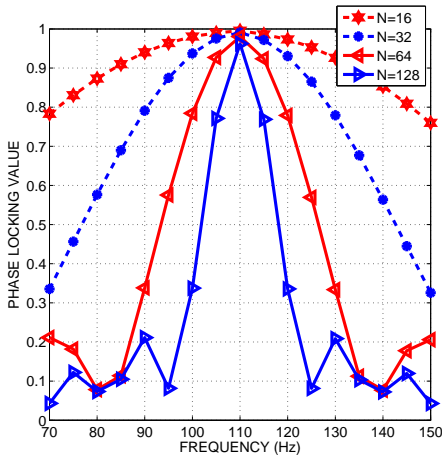


Fig. 5. Simulated PLV for different values of N (length of the FIR filters) when the frequency of one input, V_{IN1} , is held constant at 110Hz and the frequency of the other input, V_{IN0} , is swept from 70Hz to 150Hz.

are transferred to the two 32-tap moving-average FIR filters. Higher sensitivity for the PLV algorithm can be achieved by increasing the length of the FIR filters at a cost in area and complexity. Lastly, the PLV is computed by extracting the magnitude of the FIR averaged sine and cosine outputs using a 16-bit CORDIC core configured in the vectoring mode. An output multiplexer can be configured to output the instantaneous magnitude and phase of each channel, as well as the phase difference and the PLV between two channels. Each CORDIC core requires 18 clock cycles which include one clock cycle for pre-processing the angles, 16-clock cycles to perform the CORDIC algorithm and one clock cycle to output the data and post-process the angles for a total latency of 54 clock cycles to compute the PLV algorithm. The simulation results in Figure 5 show how the PLV sensitivity improves with increasing the length of the moving-average FIR filters.

IV. VLSI IMPLEMENTATION

The processor was designed and synthesized using a standard 8-metal $0.13\mu\text{m}$ CMOS technology. It contains a total of 41,366 gates and occupies an area of 0.178mm^2 . The first magnitude/phase CORDIC core occupies 20.6 percent of the area, the second sine/cosine CORDIC core uses 12.8 percent,

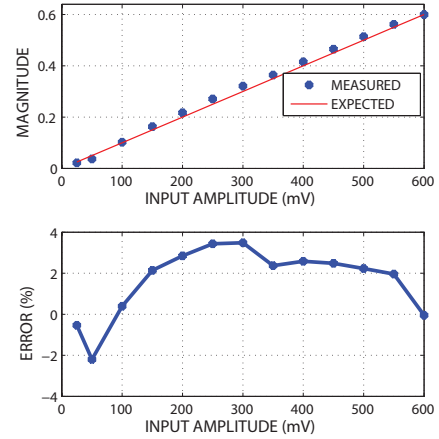


Fig. 6. (a) Experimentally measured magnitude of a sinusoidal input computed by the phase-synchronization processor. (b) The corresponding relative percent error.

the FIR moving-average filters occupy 57 percent, the third magnitude CORDIC core utilizes 9 percent and pre-processing and the output MUX occupy 1 percent of the total core area. Accuracy and sensitivity of the PLV computation can be traded for area by reducing the length of the moving-average FIR filters. A 4 times increase in the length of FIR filters yielded an overall layout area increase of 1.8 times and an overall power dissipation increase of 1.7 times.

The univariate magnitude and phase-estimation operations and the bivariate phase difference and PLV-estimation operations are all computed simultaneously for every sample and are time-multiplexed through a 10-bit output. The synthesized design can operate at frequencies above 100MHz, which is beyond the requirements of the intended application. This margin allows the ability to further reduce power dissipation by lowering the supply voltage.

V. RESULTS

A. Experimental Results

The phase-synchronization processor was prototyped in a standard $0.13\mu\text{m}$ CMOS technology and characterized experimentally. Two analog signals were digitized, sent through FIR filters to obtain the Hilbert transform and its delayed version, and fed to the processor.

The experimentally measured magnitude extraction results are shown in Figure 6, when a sinusoid is applied as an input to the processor. The maximum error is below 3.5 percent with respect to the full scale when the input is between 0mV and 600mV. For a neural amplifier gain of $2,000\text{V/V}$, this corresponds to a neural signal between $0\mu\text{V}$ and $300\mu\text{V}$.

Next, two sinusoid inputs were set to 110Hz, with one sinusoid having its phase locked while adjusting the phase of the other sinusoid. The measured phase difference between this pair of inputs is shown in Figure 7. The maximum error is approximately 1.5 percent.

The measured PLV between a pair of inputs is shown in Figure 8. The average PLV between the two inputs is computed with one input held constant at 110Hz, while the other input frequency is swept from 60Hz to 160Hz. As expected, the

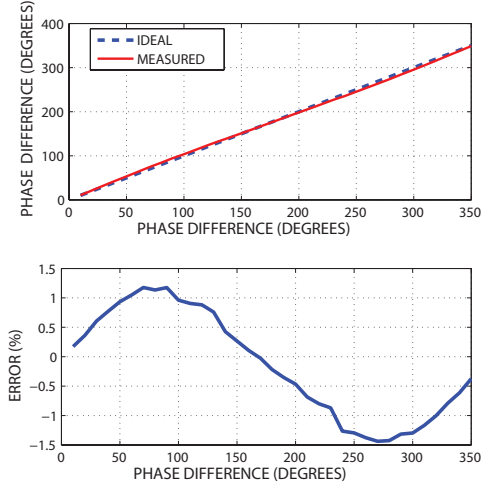


Fig. 7. Experimentally measured phase difference between two input sinusoids. (b) The corresponding relative percent error.

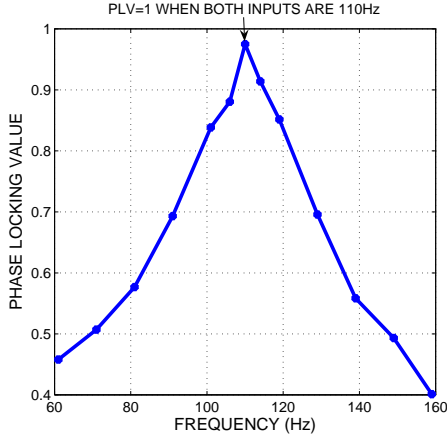


Fig. 8. Experimentally computed PLV when the frequency of one input, V_{IN1} , is held constant at 110Hz and the frequency of the other input, V_{IN0} , is swept from 60Hz to 160Hz.

computed PLV is near unity when the two signals have the same frequency. When the second signal has its frequency set to 60Hz or 160Hz, the PLV drops to 0.45 and 0.4 respectively. The phase locking sensitivity can be further improved by increasing the length of the moving-average FIR filters.

The experimentally measured power dissipation of the processor for a supply voltage of 0.85 and 1.15V operating at various clock frequencies is shown in Figure 9. For a 0.85V supply at 2.5MHz and 10MHz the processor dissipates $102\mu\text{W}$ and $412\mu\text{W}$, respectively. For a 1.15V supply at 2.5MHz and 10MHz the processor dissipates $231\mu\text{W}$ and $897\mu\text{W}$, respectively. For only one pair of channels, operating at 1.7kS/s the processor dissipates $3.6\mu\text{W}$ from a 0.85V supply. At lower clock frequencies of 39kHz and 156kHz the processor dissipates $4.6\mu\text{W}$ and $17.3\mu\text{W}$, respectively, from a 1.15V supply and $2.4\mu\text{W}$ and $8.5\mu\text{W}$, respectively, from a 0.85V supply.

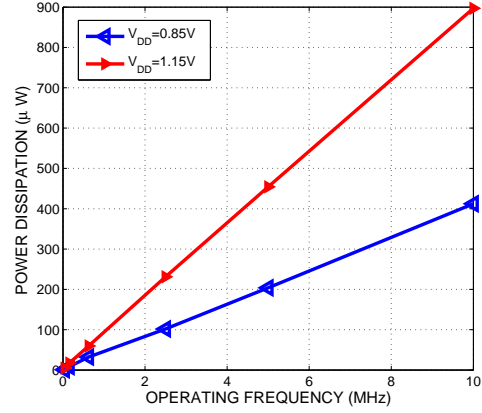


Fig. 9. Experimentally measured power dissipation at different operating frequencies.

TABLE I
EEG DATABASE USED IN VERIFICATION OF THE PHASE-SYNCHRONIZATION PROCESSOR. SEIZURE TYPES: SIMPLE PARTIAL (SP), COMPLEX PARTIAL (CP), GENERALIZED TONIC-CLONIC (GTC). SEIZURE LOCATION: HIPPOCAMPAL (H), NEOCORTICAL (NC). ELECTRODE TYPES: DEPTH (D), STRIP (S), GRID (G).

Patient	Sex	Age	Type	Location	Electrodes	Outcome	No. Seizures	EEG (hrs)	No. Channels
1	F	30	SP, CP, GTC	H	D, S	I	10	98	60
2	M	17	SP, CP, GTC	NC	G, S	I	10	30	44
3	M	10	SP, CP, GTC	H	D, S	I	10	102	22

B. Simulated Human EEG Results

A Verilog-AMS model of the phase-synchronization processor is too computationally complex to be used in early seizure detection simulations. Instead, a Simulink model which had its resolution and accuracy set to match the performance of the RTL-level implementation of the synthesized processor was utilized.

The efficacy of the phase-synchronization processor in early seizure detection was verified and validated on an EEG database from the seizure prediction project at the University of Freiburg [31]. It consists of 222 hours of intracranial EEG recording of three patients with a total of 30 seizures analyzed and labeled by certified epileptologists as summarized in Table I. The data was acquired by a Neurofile NT digital video EEG system with 128 channels, 512 Hz sampling rate, and a 16-bit analog-to-digital converter via implanted depth, strip and grid electrodes.

For each patient, three intracranial electrodes located in the proximity of an epileptic focus were used. For each electrode type, a sub-set of contact pairs was selected for the PLV computation as follows. First, only the contact pairs of the same electrode type were used as inputs to the PLV processor

to suppress common-mode noise. Next, a reference electrode was chosen for each electrode type as the contact furthest away from the epileptic focus. Then, for each contact pair, the signal spectrum was separated into five frequency bands via high-Q bandpass filters: delta (0.5-4 Hz), theta (4-8 Hz), alpha (8-13 Hz), a sub-band of beta (15-25 Hz) and gamma (30-48 Hz). Finally, a sub-set of contact pairs across all frequency bands was selected by pairing each contact with the reference and observing the channel magnitudes and the PLV within three hours of a clinical seizure onset.

The sensitivity, defined as the true positive rate (TPR), of the phase-synchronization algorithm was evaluated as a function of seizure occurrence period (SOP), seizure prediction horizon (SPH), false positive rate (FPR) and maximum false positive rate (FPR_{max}) [22], [23], [24]. The SOP is defined as the period of time in which only one seizure is to be expected. It was varied between 5 and 40 minutes to account for the uncertainty in the seizure frequency. The SPH was set to between 16 seconds and 5 minutes to allow enough time for the therapeutic intervention, such as electrical stimulation or a warning signal to the patient.

Three early seizure detection methods were used in the analysis of the EEG database: magnitude, PLV and combined magnitude with PLV detectors. The magnitude detector is active when the amplitudes of both input channels within a frequency band of interest cross their corresponding thresholds. The PLV detector is triggered when the phase locking value, integrated over an adjustable period of time, drops below a certain threshold. The combined magnitude and PLV detector output is formed by AND-ing the outputs of the individual detectors. Each threshold detector, once triggered, remains active for the duration equal to the sum of SOP and SPH time periods. All early seizure detection methods were compared against the random detector.

The experimental results showed highest PLV activity in the 15-25Hz frequency band. Figure 10 presents an example of an early seizure detection result computed by the phase-synchronization processor in the 15-25Hz frequency band for patient 2. The clinical seizure onset is characterized by an increase in the magnitude and a marked fluctuation (a drop in this case) in the PLV before the seizure. The phase locking value reaches 1 during the seizure reflecting the synchronized firing of neurons. Similar early seizure detector outputs generated by the processor are observed in the 15-25Hz frequency band of patient 3 as shown in Figure 11. The magnitude and PLV thresholds are adjusted for each patient to achieve the highest sensitivity in early detection of seizures.

Figures 12(a) and 12(b) show the variation of the sensitivity with FPR and SOP , respectively, for patient 2 in the University of Freiburg data set. Each plot compares the sensitivity of the three detectors in comparison to a random detector. The sensitivity plot in Figure 12(a) shows that the best detector, the PLV detector, achieves 66 percent sensitivity with FPR of 0.65 FP/hr, SOP of 30 minutes, and SPH of less than 5 minutes.

The sensitivity plot in Figure 12(b) shows that when the FPR_{max} is increased to 1.2/hr, the true positive rate reaches 100 percent for a seizure occurrence period greater than

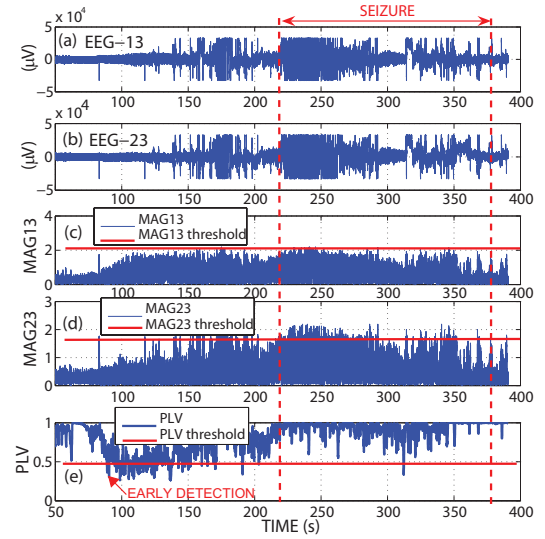


Fig. 10. Early seizure detection results example for patient 2. (a), (b) Two input intracranial EEG signals recorded on electrodes 13 and 23, respectively. (c), (d) Magnitude of the signals shown in (a), (b), respectively, after they are bandpass filtered in the 15Hz to 25Hz frequency range, computed by the prototyped phase-synchronization processor. (e) Integrated PLV between the two inputs in the 15Hz to 25Hz frequency band computed by the prototyped phase-synchronization processor.

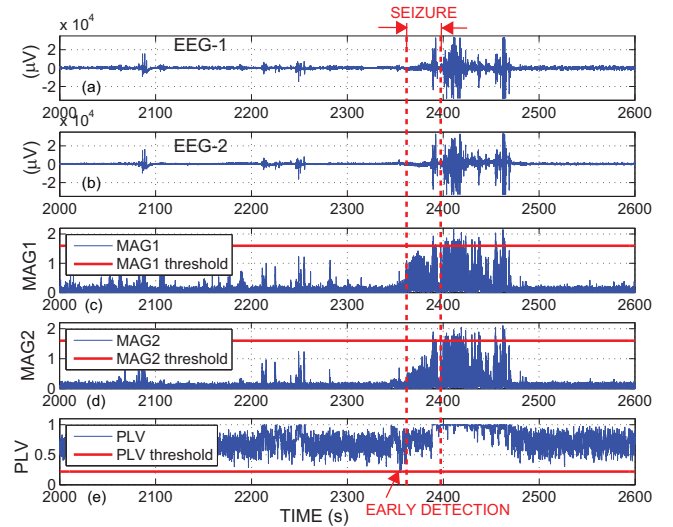


Fig. 11. Early seizure detection results example for patient 3. (a), (b). Two input intracranial EEG signals recorded on EEG electrodes 1 and 2, respectively. (c), (d) Magnitude of the signals shown in (a), (b), respectively, after they are bandpass filtered in the 15Hz to 25Hz frequency range, computed by the prototyped phase-synchronization processor. (e) Integrated PLV between the two inputs in the 15Hz to 25Hz frequency band computed by the prototyped phase-synchronization processor.

10 minutes. By increasing the FPR_{max} to 1.2 FP/hr-2.0 FP/hr depending on a patient, TPR approaches 100 percent for all patients. The FPR_{max} could not always be made constant by varying the thresholds; therefore, the average FPR_{max} rates are shown for each early detection method in Figure 12(b).

The sensitivity results in early seizure detector are comparable to previously reported software-based bivariate prediction algorithms [22], [23], [24] as summarized in Table II (with the exception of [22] which results in 100 percent TPR at $FPR=1/hr$ versus 100 percent TPR at $FPR=1.2/hr$ performance yielded by the presented phase-synchronization processor architecture). All of the listed algorithms have been tested on the same benchmark data set from the University of Freiburg, but the presented algorithm is the only one that has been implemented as a low-power implantable integrated circuit. Recent integrated circuit seizure detector implementations [19], [20], [32] achieve a high TPR for a given set of patient seizure data, but have not been tested on publicly available benchmarking human seizure data sets such as the one from University of Freiburg and have lower detection-to-seizure-onset times as shown in Table II.

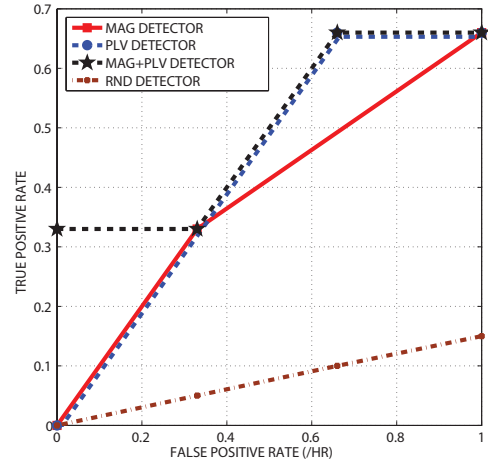
C. Experimental Human EEG Results

Two-electrode intracranial EEG data from patient 1 from University of Freiburg database was loaded onto a dual-channel Tektronix AFG3252 arbitrary waveform generator and fed into the phase-synchronization processor chip. A bandpass filter filtered the inputs to 15-25Hz frequency band. Two 8-bit ADCs and four 16-tap FIR filters (two all-pass and two Hilbert filters) digitized and applied a 90 degree phase shift, respectively, to the two signals. The processor simultaneously computed both magnitudes, the phase difference and the PLV at 1.7kS/s dissipating $3.6\mu W$ from a 0.85V supply.

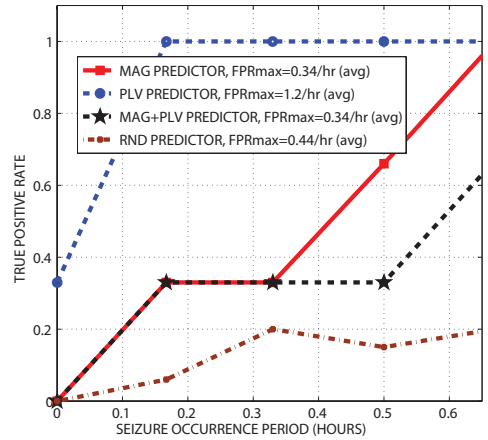
Two-electrode intracranial EEG seizure recordings from patient 1 (electrode-40 and electrode-44) are shown in Figure 13(a) and (b). Figure 13(c) shows the experimentally measured magnitude from electrode-40, while Figure 13(d) shows the the experimentally measured magnitude from electrode-44. For both inputs, the experimentally measured magnitude was observed to increase during the seizure. Lastly, Figure 13(e) shows the experimentally measured PLV between the two inputs. The PLV was observed to drop 15 seconds before the onset of the seizure displaying an early detection, then increasing during the seizure. Seizure data from other patients were also fed into the processor. The magnitude was observed to increase before and during the seizure while a pronounced fluctuation of PLV is observed before and during the seizure.

VI. CONCLUSIONS

A compact low-power signal processing VLSI architecture has been presented that computes the phase locking value on two neuroelectrical signals and the instantaneous magnitude on individual neural inputs. The signal processor is used in conjunction with a neural recording front-end and operates in real time on frequency bands in the neural spectrum. The processor occupies $0.178mm^2$ area and dissipates $3.6\mu W$ operating on a pair of inputs sampled at 1.7kS/s from a 0.85V



(a)



(b)

Fig. 12. Early seizure detection results for patient 2, showing (a) true positive rate vs. false positive rate plot with the seizure occurrence period held at 30min, and (b) true positive rate vs. seizure occurrence period plot. For the above detectors, MAG refers to magnitude, PLV refers to phase locking value, and RND refers to random.

supply. Results from pre-recorded human intracranial EEG data demonstrate the effectiveness of the processor in early seizure detection.

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TABLE II
PERFORMANCE COMPARATIVE ANALYSIS OF BIVARIATE SEIZURE DETECTION AND PREDICTION ALGORITHMS.

Seizure Detection and Prediction Methods			TPR vs FPR (%) for SOP=30min		TPR vs SOP (%) for FPR < 1.2/hr		Avg. Detection to-Seizure-onset
Reference	Method	Type	FPR=0/hr	FPR=1/hr	SOP=10m	SOP=40m	
[22]*	Phase Locking Value	Software	20	100	20	100	11 min
[23]*	Similarity Index	Software	30	40	20	30	5 min
[33]*	Correlation Dimension	Software	15	40	15	70	11 min
[19]	Event Threshold	IC	-	94	-	-	8.5 s
[20]	SVM Classifier	IC	-	82	-	-	7.5 s
[32]	Modulated Treshold	IC	-	-	-	-	13.5 s
This Work*	Phase Locking Value	IC	33	66	33	100	59 s

TPR: true positive rate, FPR: false positive rate, SOP: seizure occurrence period. * Based on Freiburg EEG Database [31].

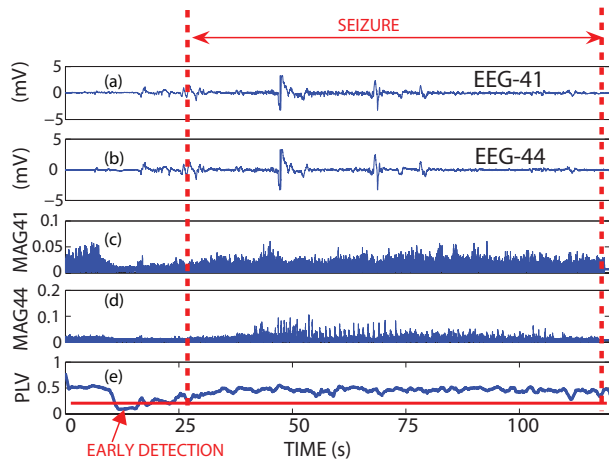


Fig. 13. Experimentally measured early seizure detection results for patient 1. (a), (b). Two inputs recorded from intracranial EEG electrodes. (c) Experimentally measured magnitude in the 15-25Hz range of the signal shown in (a). (d) Experimentally measured magnitude in the 15-25Hz range of the signal shown in (b). (e) Experimentally measured PLV between signals in (a) and (b).

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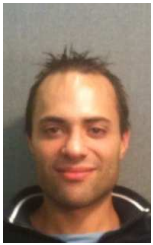
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Karim Abdelhalim (S’06) received the B.Eng. and M.A.Sc. degrees in Electrical Engineering from Carleton University, in Ottawa, Canada, in 2005 and 2007, respectively. His M.A.Sc. thesis focused on the implementation of an ultra low power ADC for biomedical applications.

He is currently working toward the Ph.D. degree in Electrical and Computer Engineering at the University of Toronto. His research interests are in the area of wireless closed-loop implantable SoCs for neural interfaces. From July 2010 to October 2010,

he worked as a mixed-signal design engineering intern at Broadcom Corp, Irvine, CA.

He is a recipient of the Alexander Graham Bell Canada Graduate Scholarship awarded by the Natural Sciences and Engineering Research Council of Canada (NSERC) from 2007 to 2010. He has also held the Ontario Graduate Scholarship (OGS) in 2005, the NSERC CGS-M in 2006 and the Ontario Graduate Scholarships in Science and Technology (OGSST) in 2011. He also worked as a volunteer at the International Solid-State Circuits Conference (ISSCC) from 2008-2011.



Vadim Smolyakov (S’05) received the B.A.Sc. degree with honors in engineering science specializing in electrical engineering from the University of Toronto, Toronto, ON, Canada in 2009, where he is currently pursuing the M.A.Sc. degree in electrical and computer engineering.

Mr. Smolyakov held numerous research assistant positions within electrical and computer engineering department at the University of Toronto. From May 2007 to August 2008, he worked as an ASIC engineer on a video processing system-on-chip at

Silicon Optix Inc, Toronto, ON. From January 2011 to July 2011, he worked as a communication systems engineer on a cross-level optimization of a system-on-chip OFDM receiver at MaxLinear Inc, Carlsbad, CA. His research interests include signal processing algorithms and VLSI architectures for digital communications, multimedia and biomedical applications.

Mr. Smolyakov is a recipient of the Natural Sciences and Engineering Research Council of Canada (NSERC) post graduate scholarship as well as the Ontario Graduate Scholarship (OGS). He has several publications in international conferences and a pending U.S. patent. He was an instructor for the Da Vinci Engineering Enrichment Program (DEEP) at the University of Toronto and a volunteer at the International Solid-State Circuits Conference (ISSCC) in 2010.



Roman Genov (SM’96-M’02) received the B.S. degree (first rank) in Electrical Engineering from Rochester Institute of Technology, NY in 1996, and the M.S. and Ph.D. degrees in Electrical and Computer Engineering from Johns Hopkins University, Baltimore, MD in 1998 and 2002 respectively.

Dr. Genov held engineering positions at Atmel Corporation, Columbia, MD in 1995 and Xerox Corporation, Rochester, NY in 1996. He was a visiting researcher in the Laboratory of Intelligent Systems at Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland in 1998 and in the Center for Biological and Computational Learning at Massachusetts Institute of Technology, Cambridge, MA in 1999. He is presently an Associate Professor in the Department of Electrical and Computer Engineering at the University of Toronto, Canada. His research interests include analog and digital VLSI circuits, systems and algorithms for energy-efficient signal processing with applications to electrical, chemical and photonic sensory information acquisition, biosensor arrays, brain-silicon interfaces, parallel signal processing, adaptive computing for pattern recognition, and implantable and wearable biomedical electronics.

Dr. Genov received Canadian Institutes of Health Research (CIHR) Next Generation Award in 2005, Brian L. Barge Award for excellence in microsystems integration in 2008, DALSA Corporation Award for excellence in microsystems innovation in 2006 and 2009, and Best Paper Award on sensors and Best Student Paper Award, both at *IEEE International Symposium on Circuits and Systems* in 2009. He is an Associate Editor of *IEEE Transactions on Biomedical Circuits and Systems*, *IEEE Transactions on Circuits and Systems-II: Express Briefs* and *IEEE Signal Processing Letters*.